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Choi et al.(54) **ORGANIC ELECTROLUMINESCENCE
DISPLAY PANEL****Publication Classification**(51) **Int. Cl.⁷** **H01L 31/109**(52) **U.S. Cl.** **257/200**(76) **Inventors:** **Beohm-Rock Choi**, Seoul (KR);
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(57) **ABSTRACT**

According to an aspect of the present invention, an organic electro-luminescence display panel is provided, which includes: an insulating substrate; a polysilicon layer formed on the substrate; a first insulating layer formed on the polysilicon layer; a gate wire formed on the first insulating layer; a second insulating layer formed on the gate wire; a data wire formed on the second insulating layer and including first and second portions; a pixel electrode connected to the first portion of the data wire; a partition defining an area on the pixel electrode; an organic light emitting member formed in the area on the pixel electrode; a common electrode formed on the light emitting member; and a planar supply voltage electrode disposed between the pixel electrode and the substrate and connected to the second portion of the data wire.

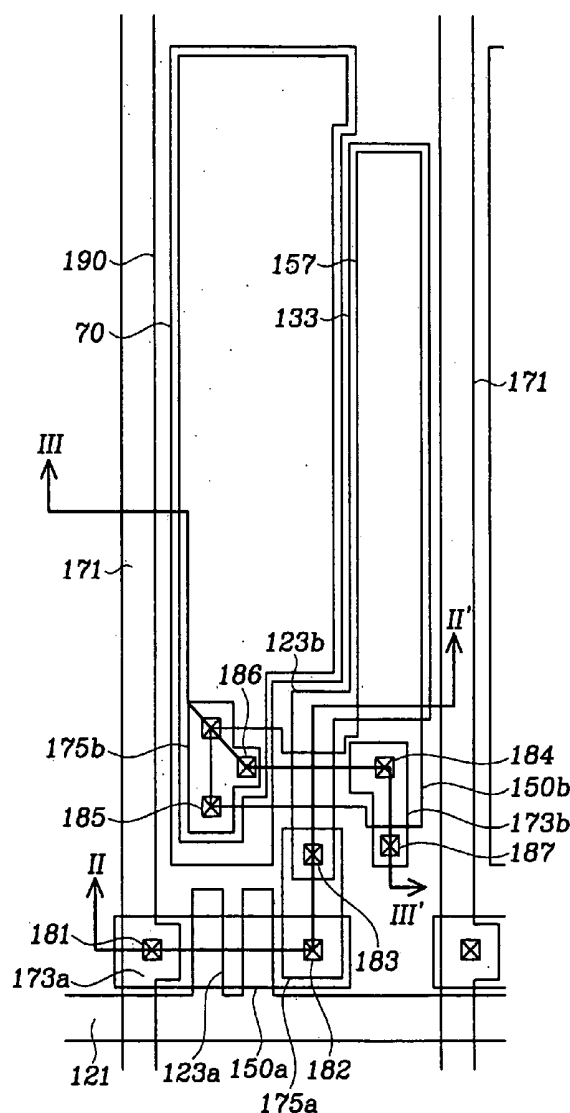


FIG. 1

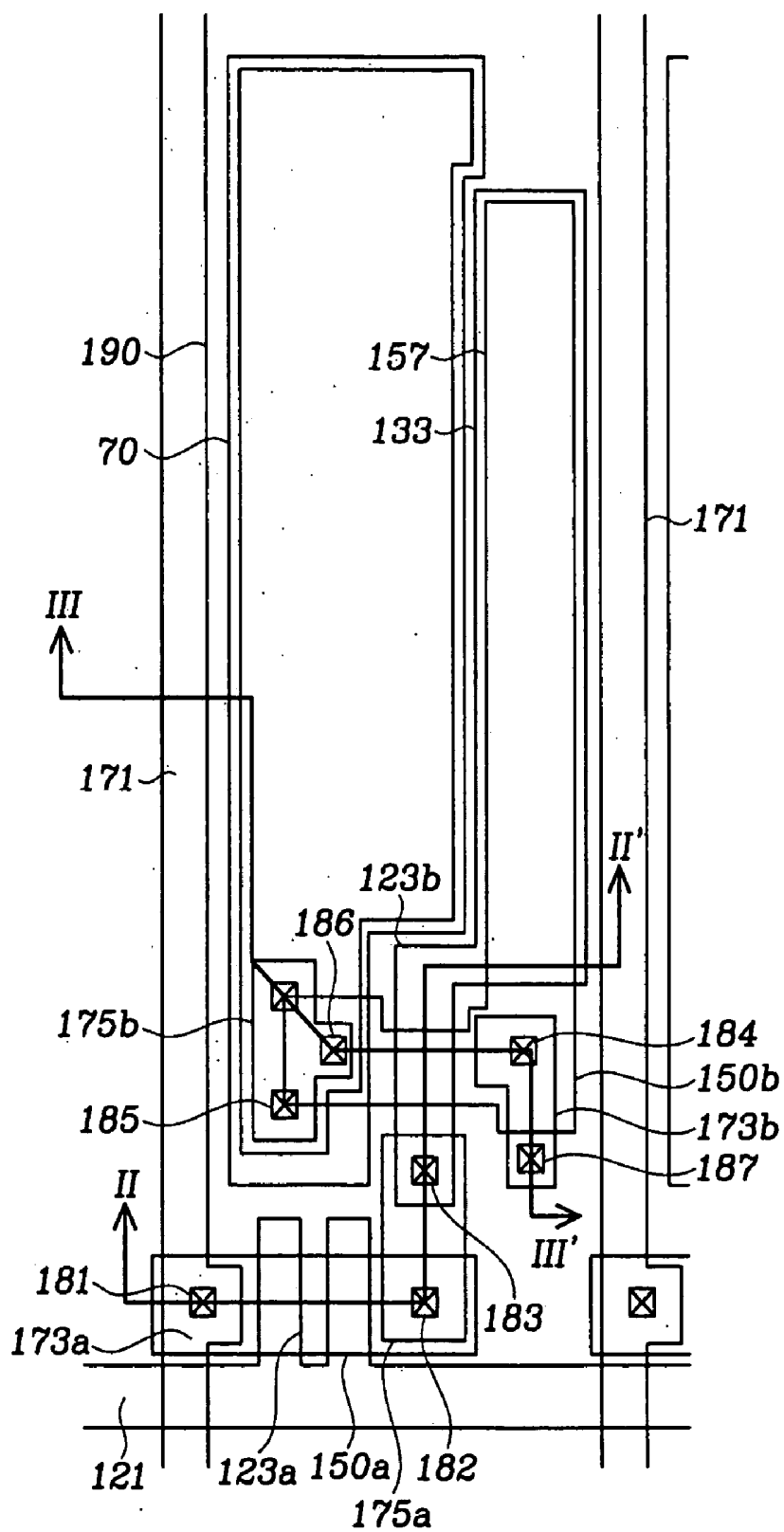


FIG. 2

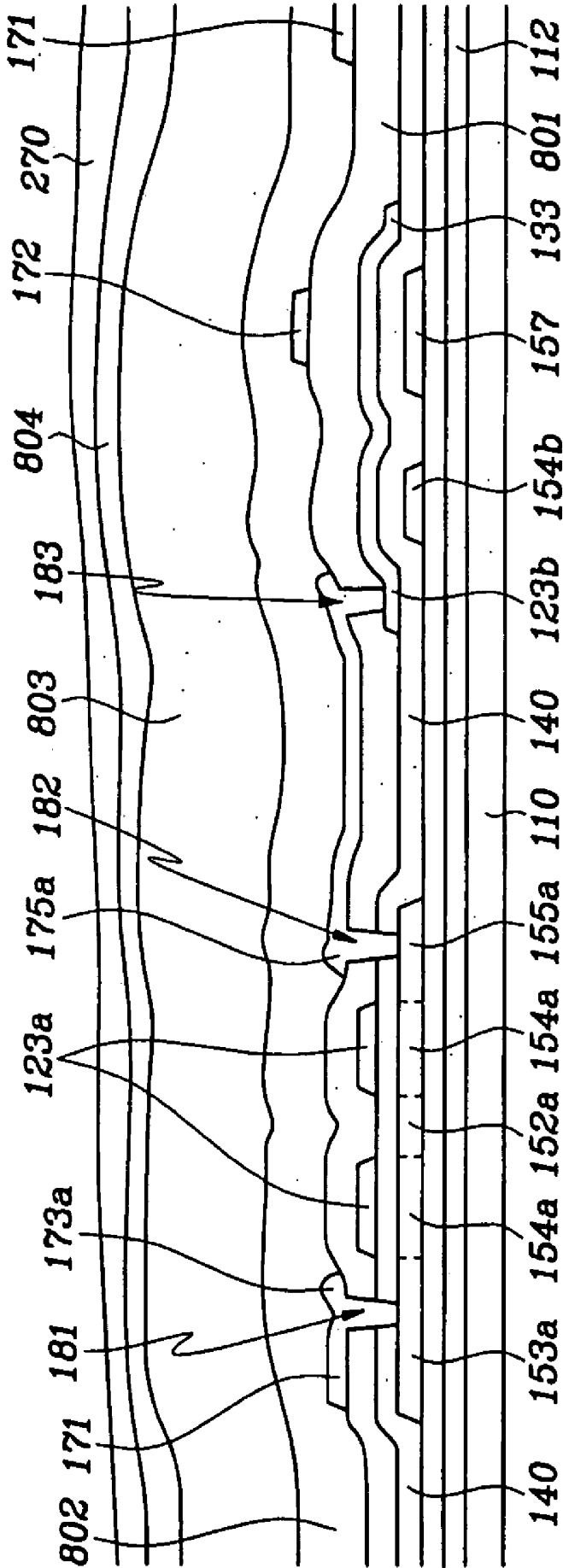


FIG. 3

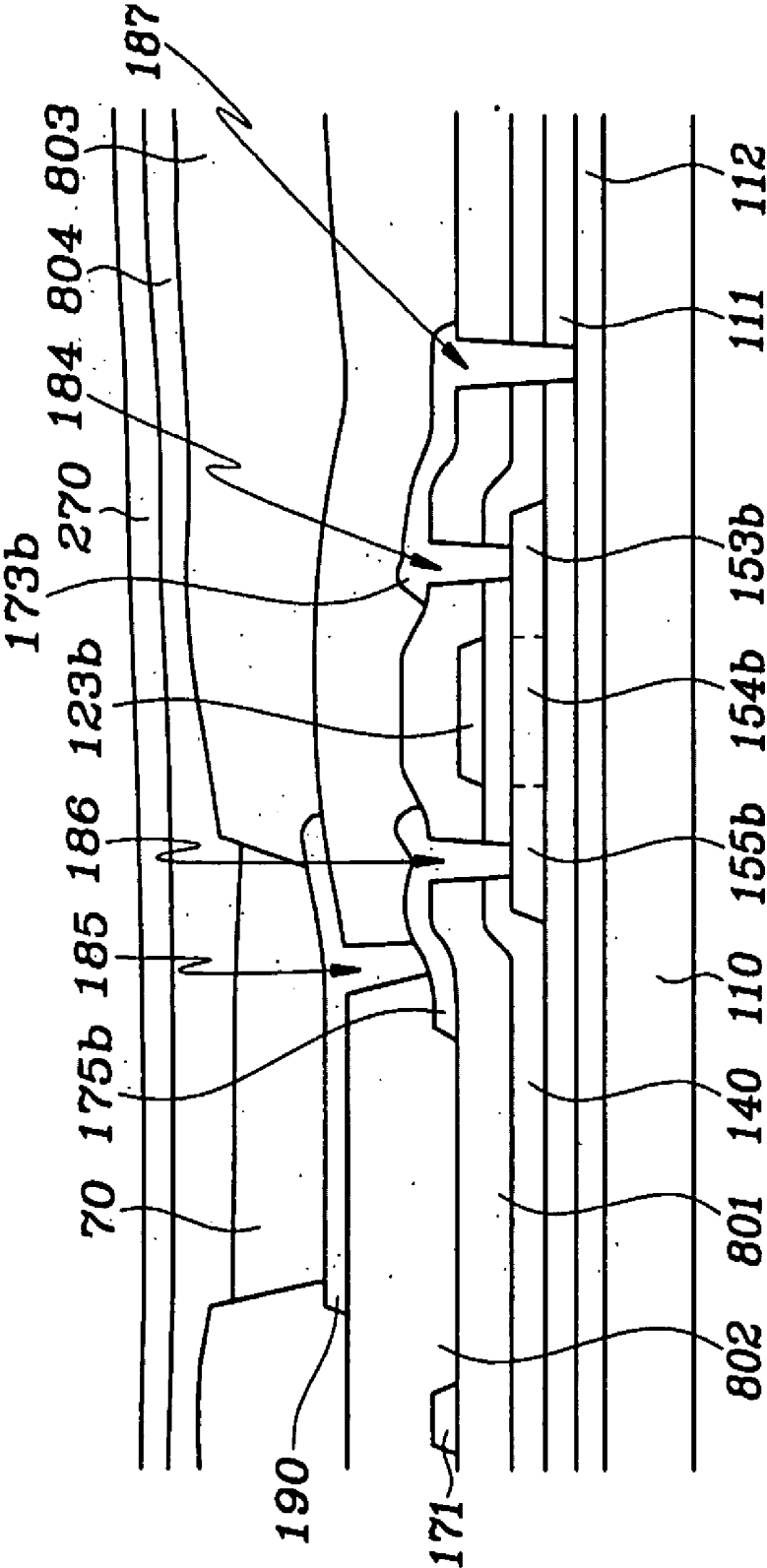


FIG. 4A

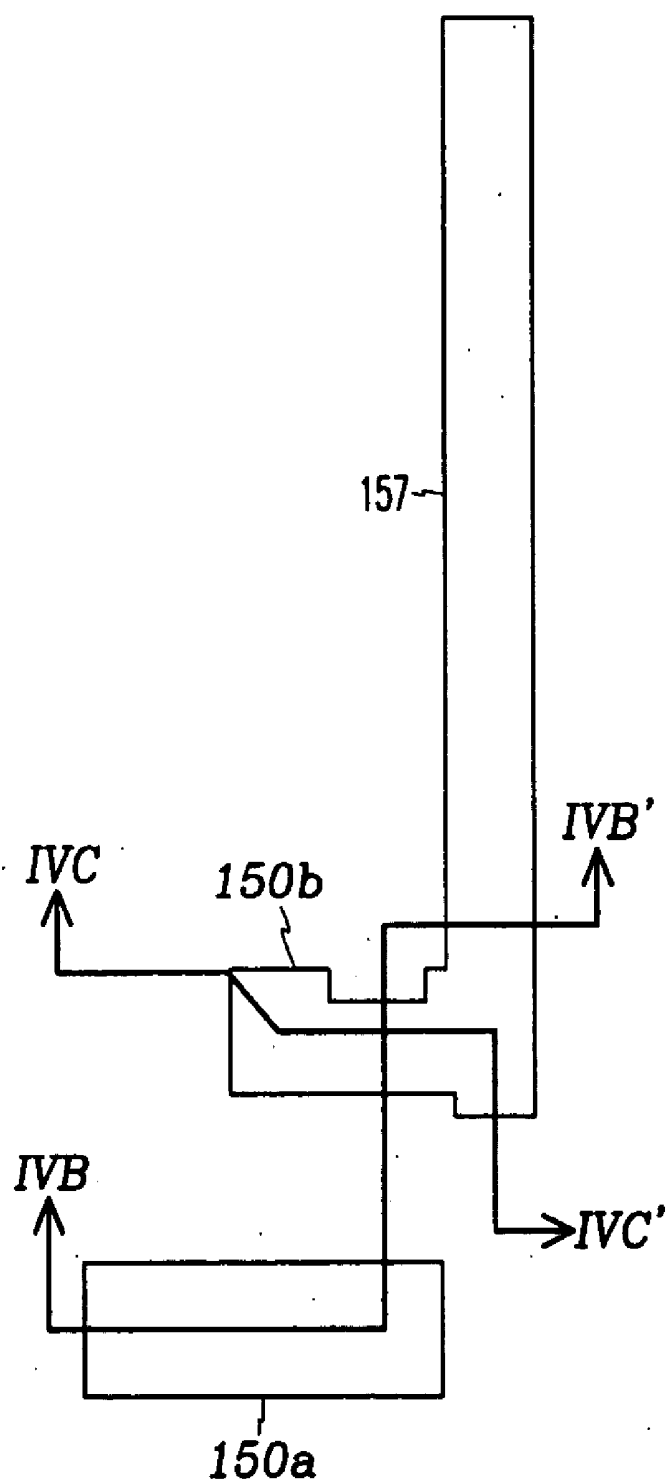


FIG. 4B

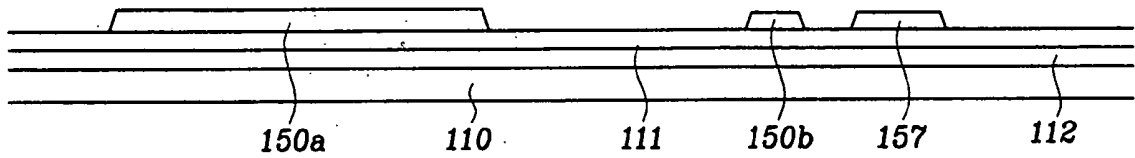


FIG. 4C

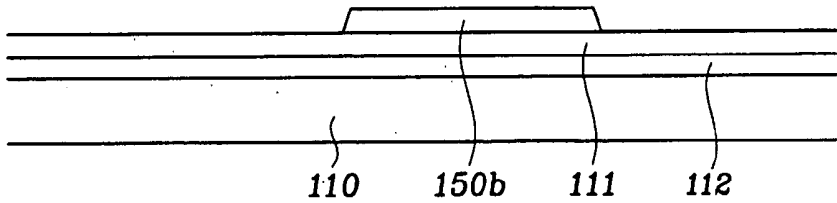


FIG. 5A

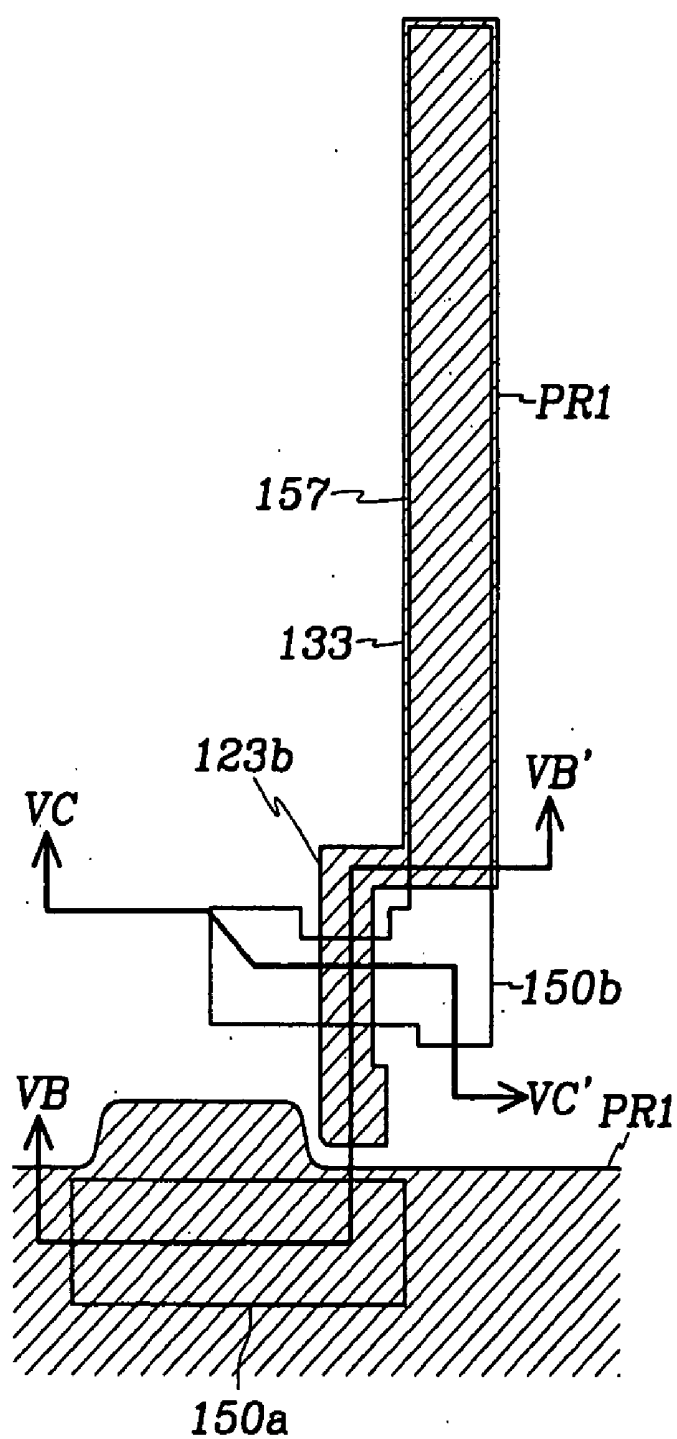


FIG. 5B

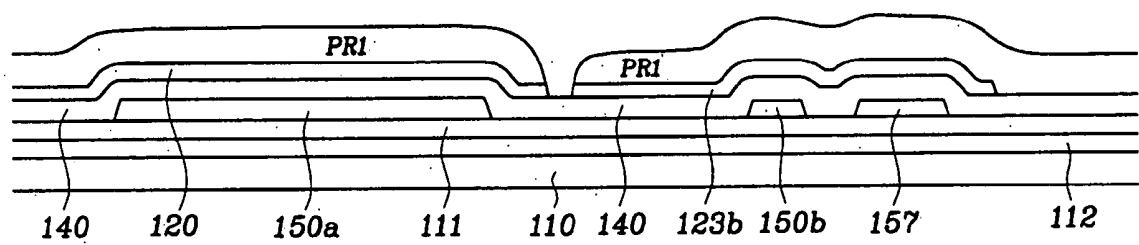


FIG. 5C

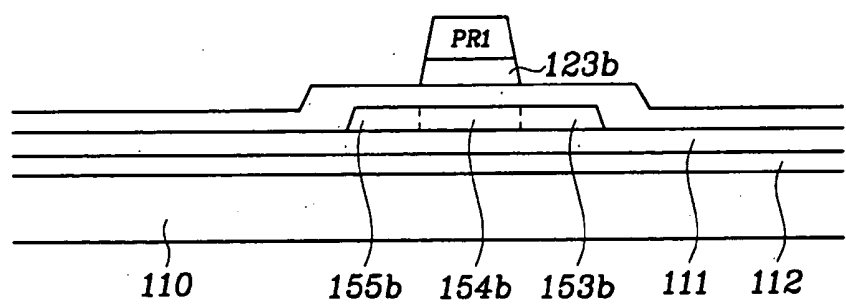


FIG. 6A

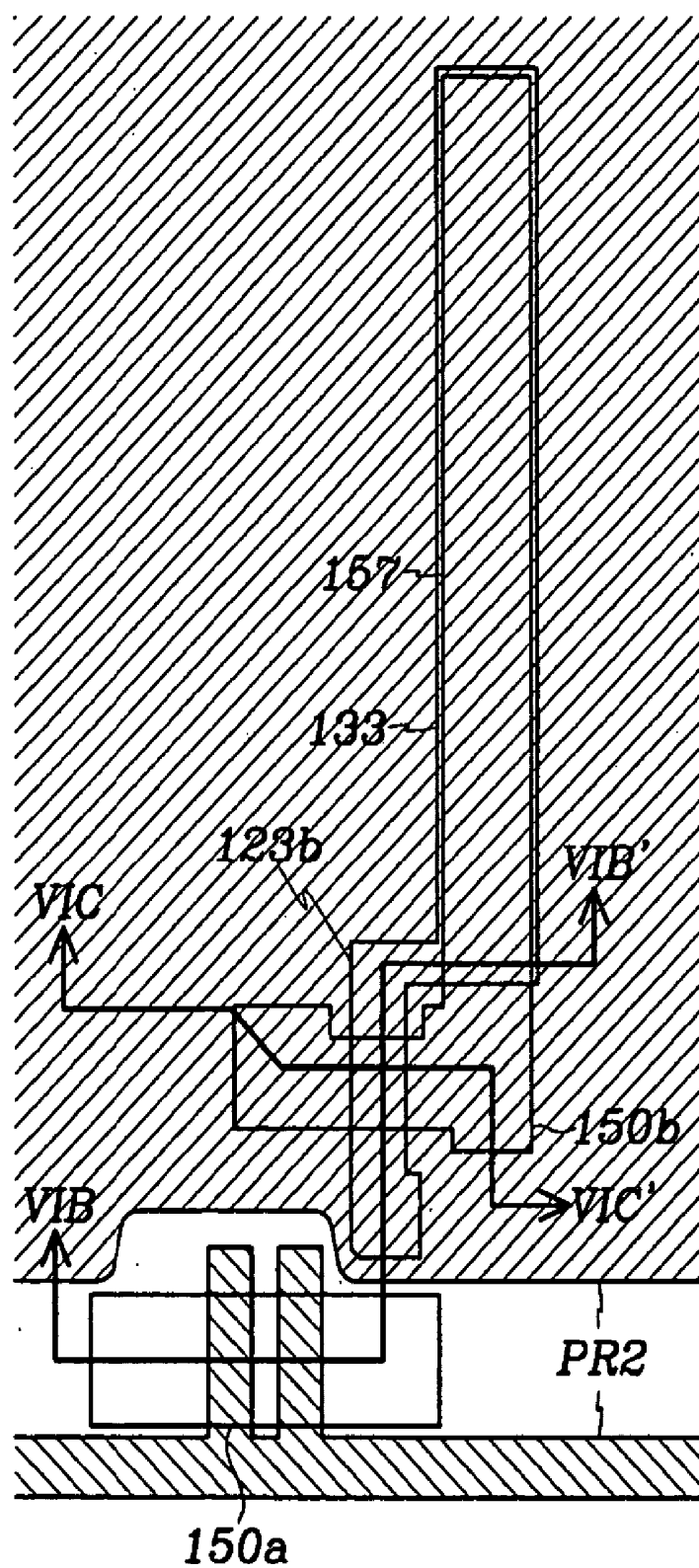


FIG. 6B

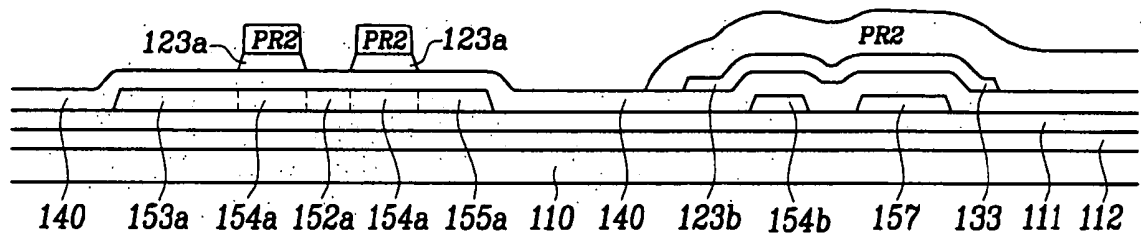


FIG. 6C

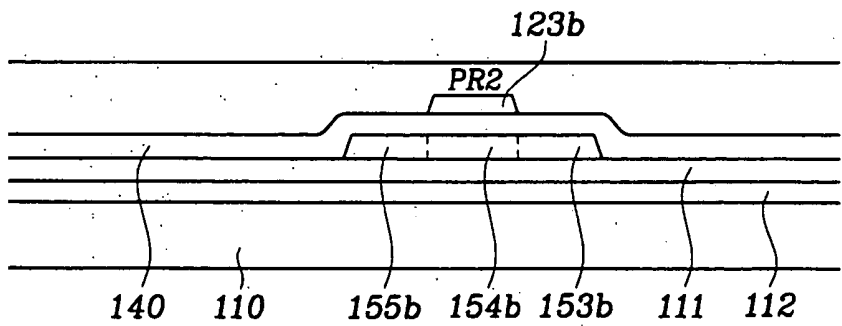


FIG. 7A

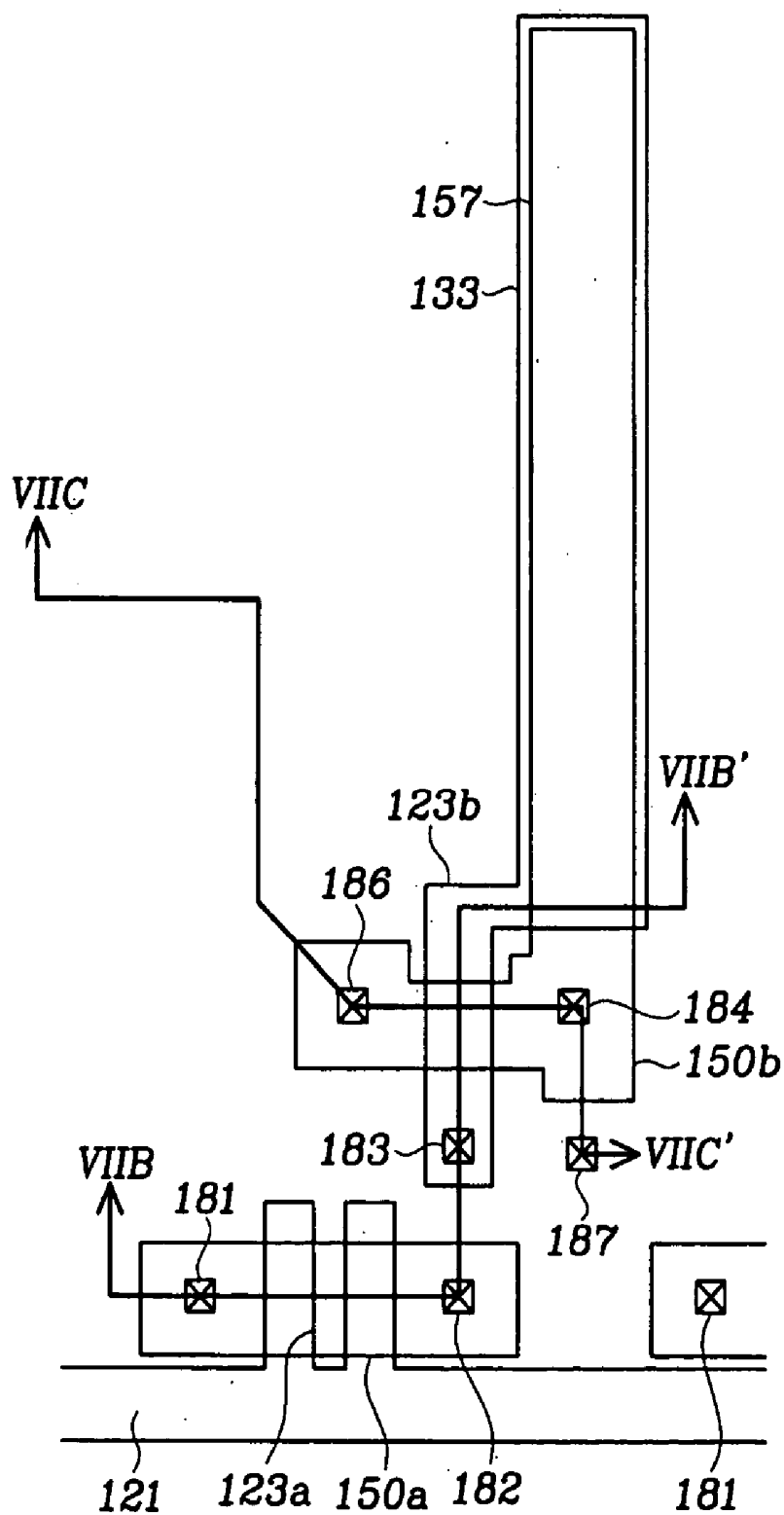


FIG. 7B

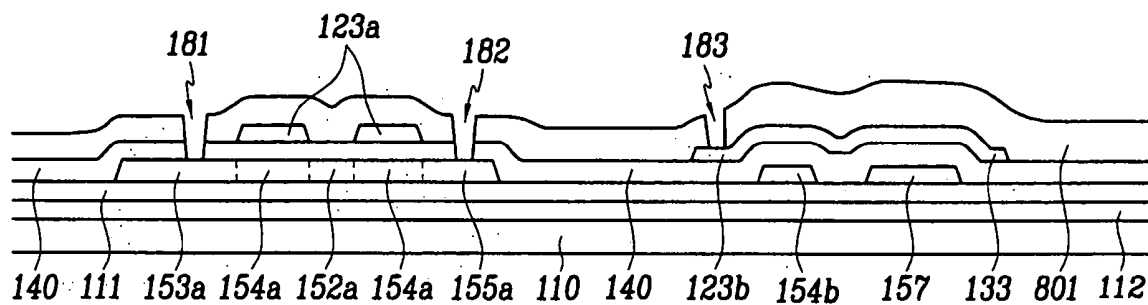


FIG. 7C

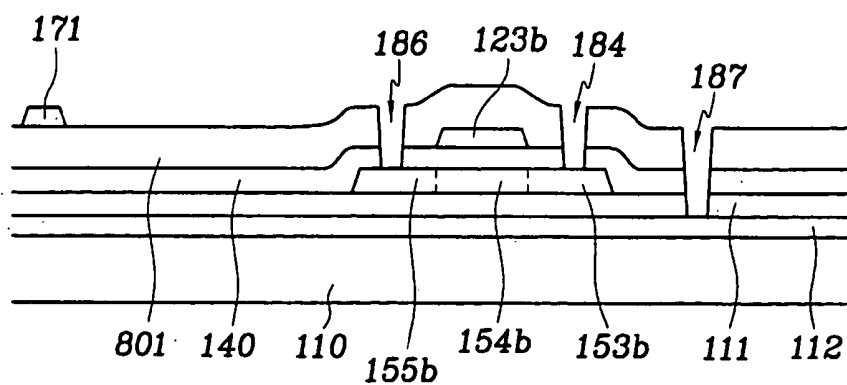


FIG. 8A

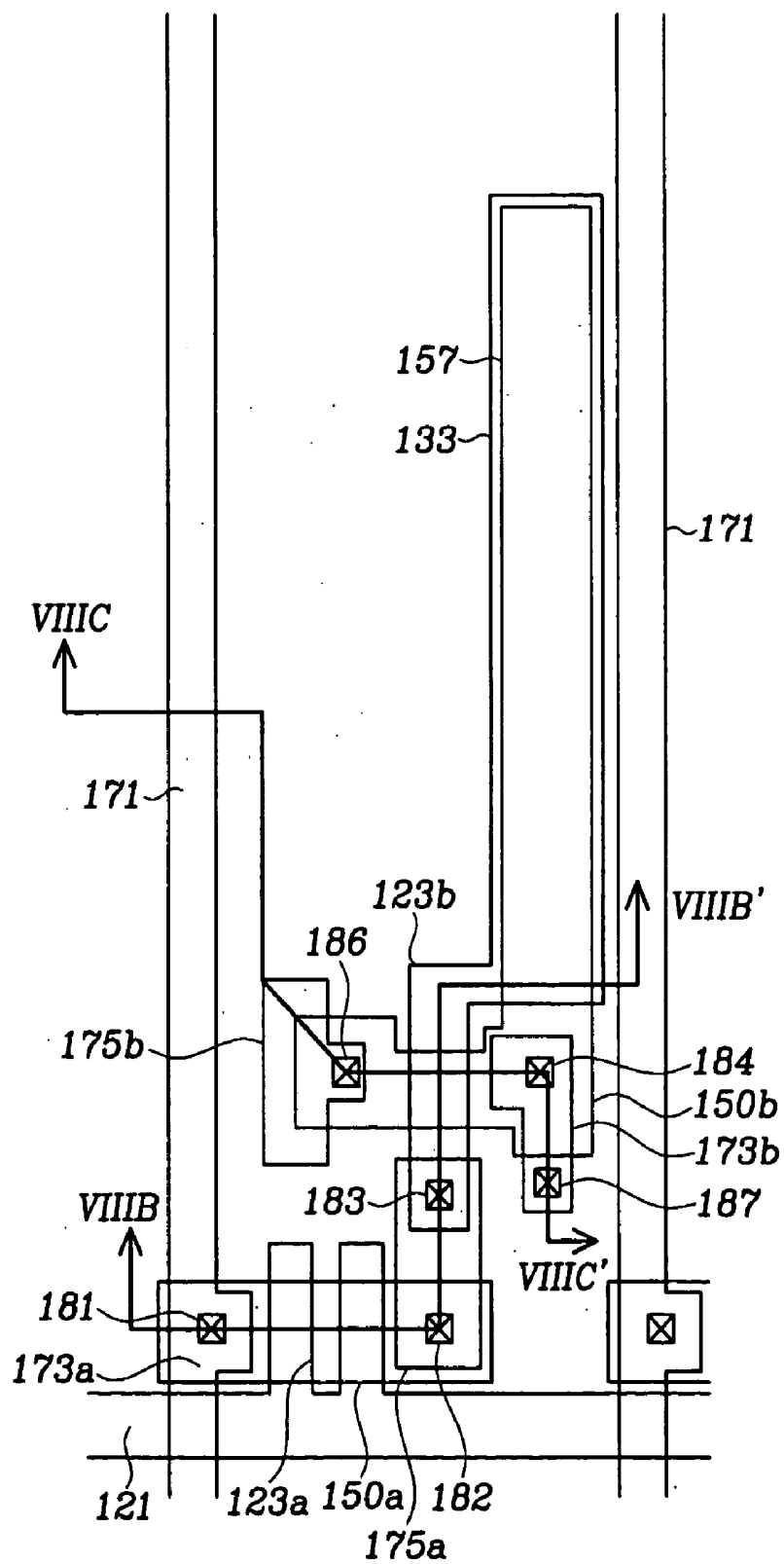


FIG. 8B

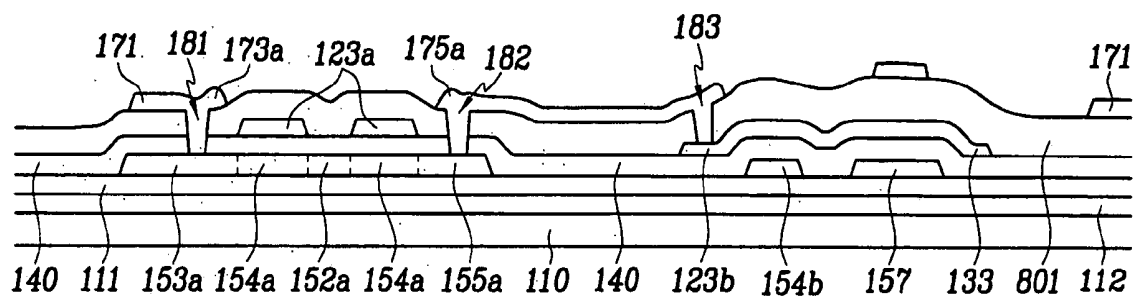


FIG. 8C

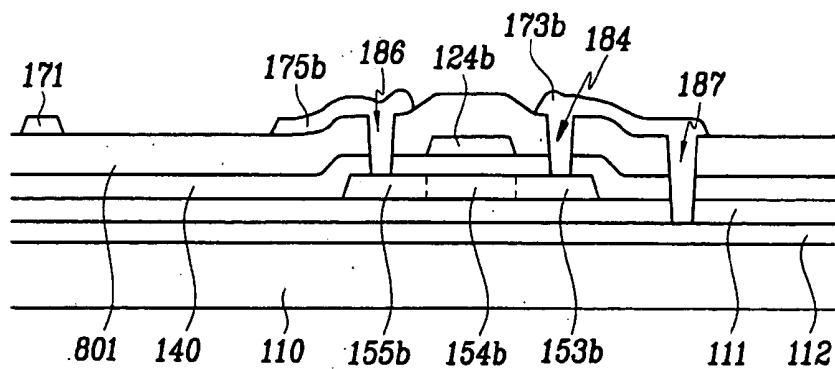


FIG. 9A

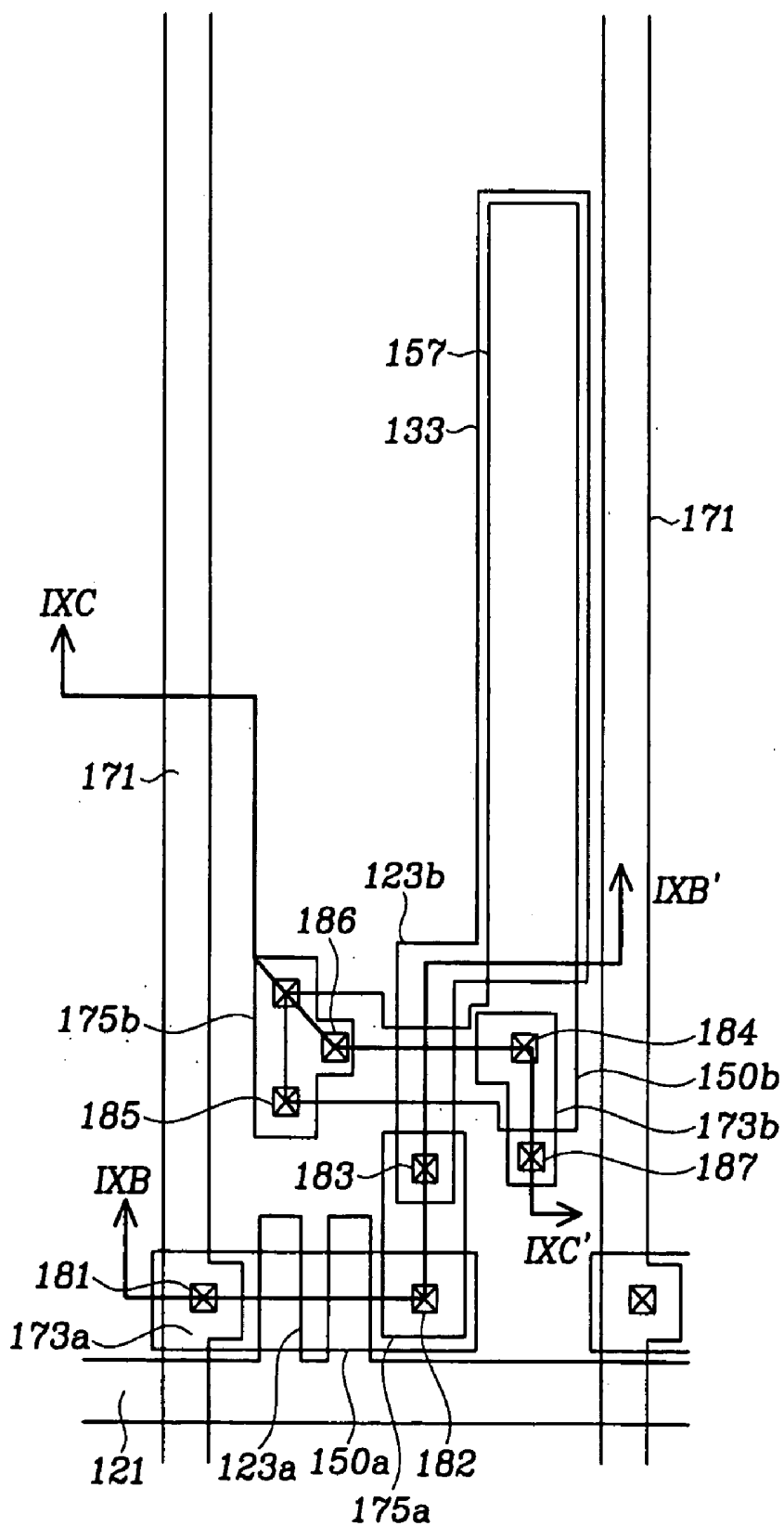


FIG. 9B

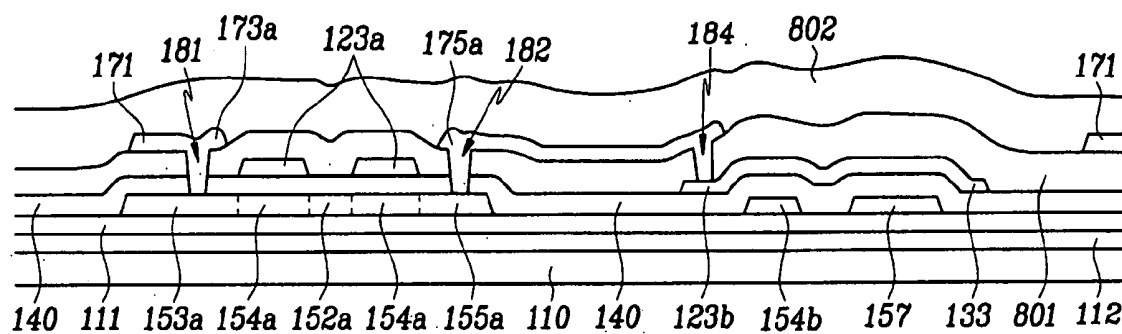


FIG. 9C

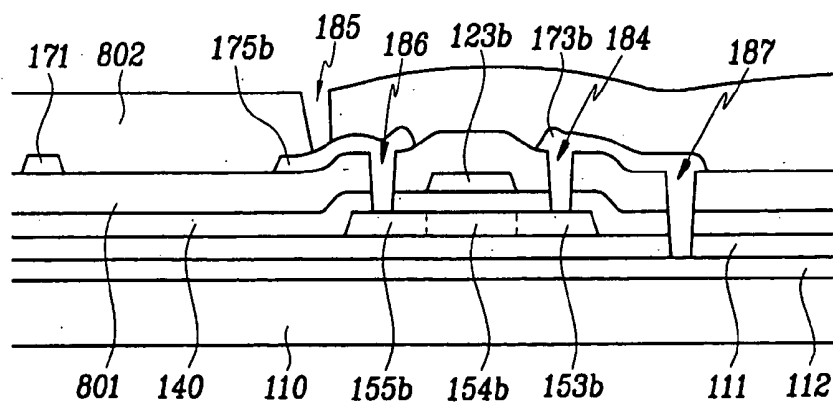


FIG. 10A

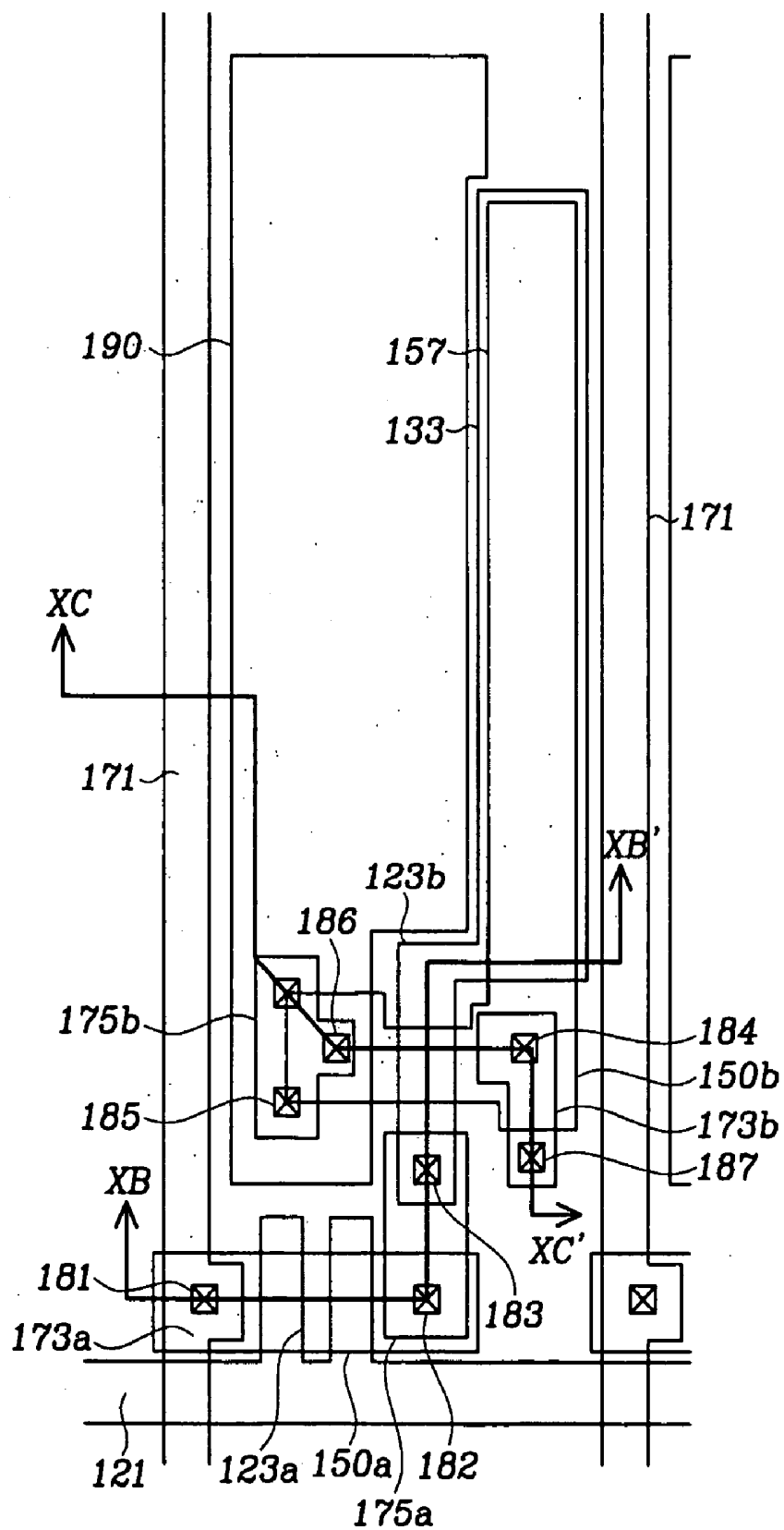


FIG.10B

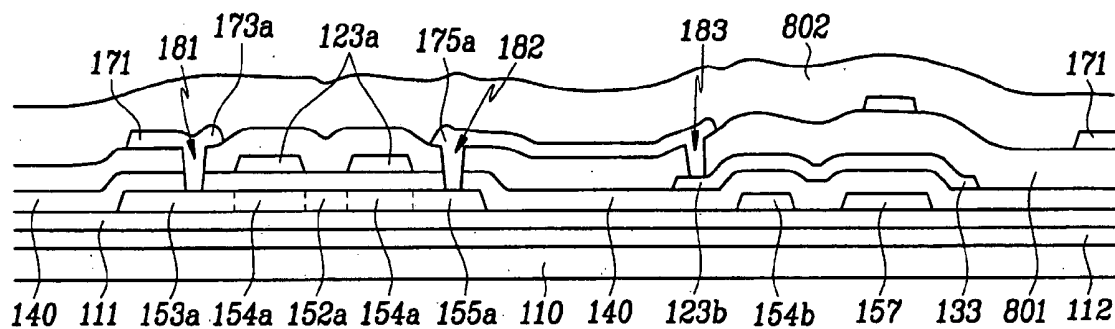


FIG.10C

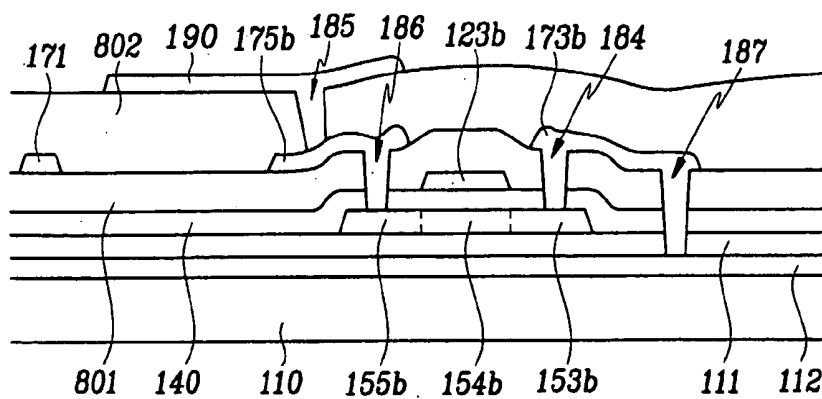


FIG. 11

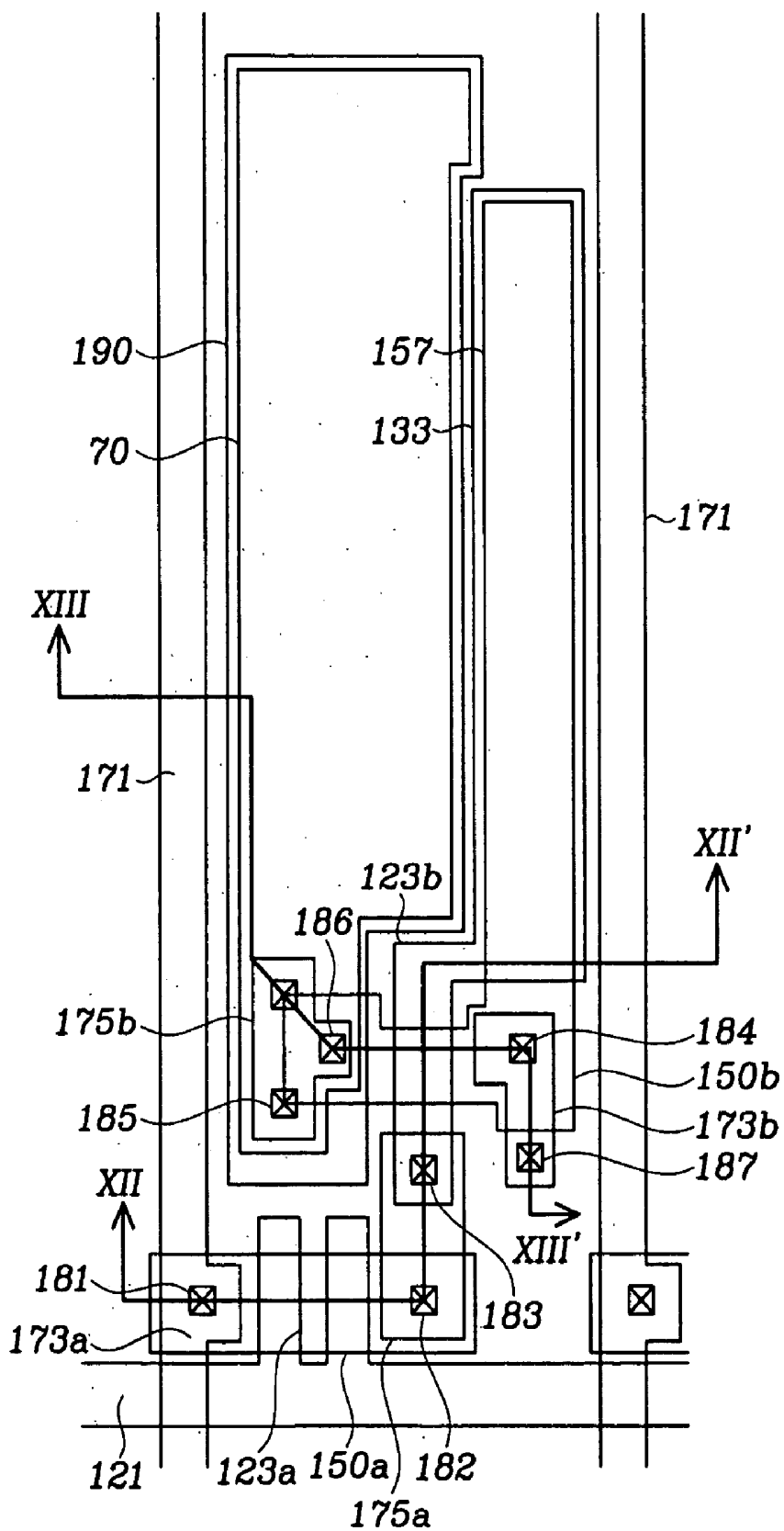


FIG. 12

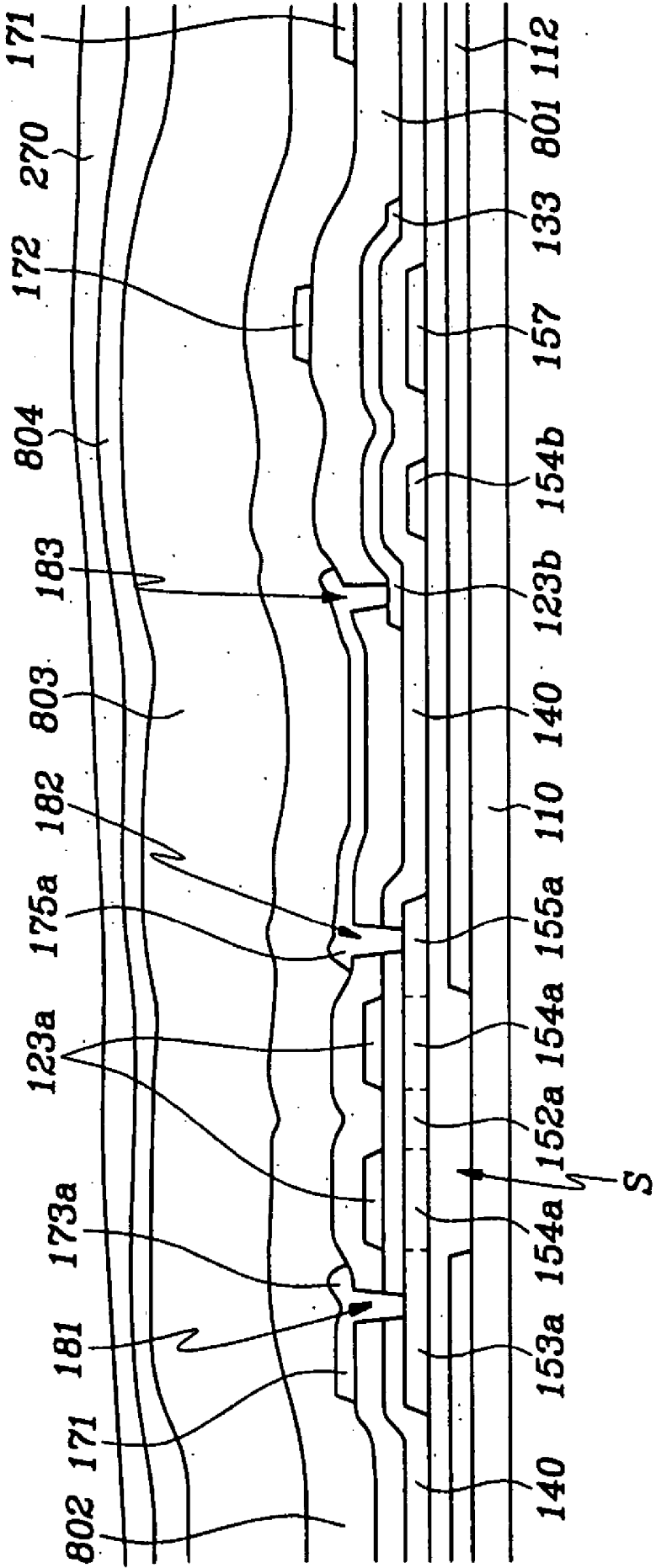
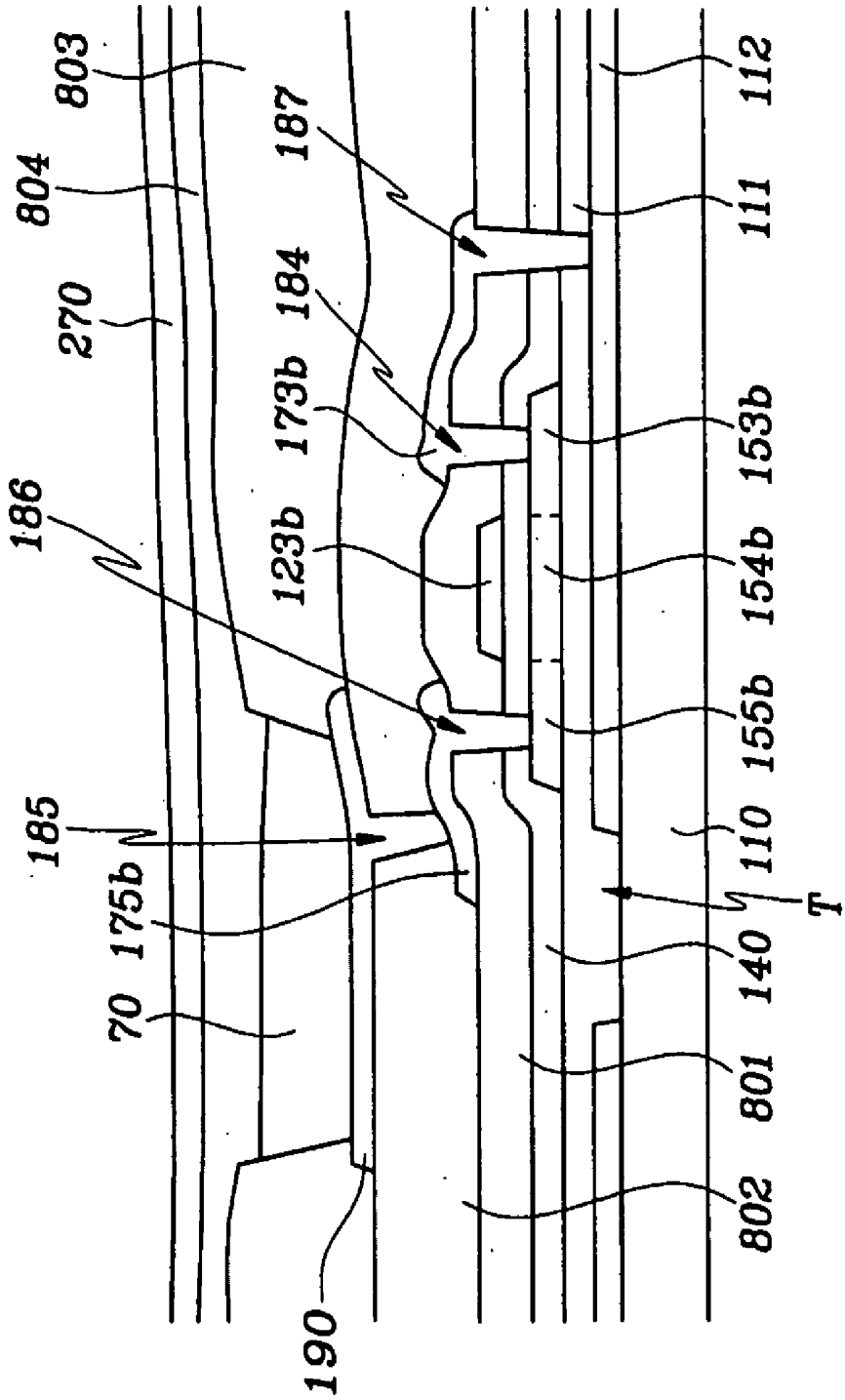


FIG. 13



ORGANIC ELECTROLUMINESCENCE DISPLAY PANEL

BACKGROUND OF THE INVENTION

[0001] (a) Field of the Invention

[0002] The present invention relates to an organic electroluminescence display panel.

[0003] (b) Description of the Related Art

[0004] Generally, an organic electro-luminescence (EL) display is a self emissive display device, which displays images by exciting an emissive organic material to emit light. The organic EL display includes an anode (hole injection electrode), a cathode (electron injection electrode), and an organic light emission layer interposed therebetween. When the holes and the electrons are injected into the light emission layer, they are recombined and pair annihilated with emitting light. The light emission layer further includes an electron transport layer (ETL) and a hole transport layer (HTL) as well as an electron injecting layer (EIL) and a hole injecting layer (HIL) for enhancing the light emission.

[0005] A plurality of pixels of the organic EL display, each including an anode, a cathode, and a light emission layer, are arranged in a matrix and driven in passive matrix (or simple matrix) addressing or active matrix addressing.

[0006] The passive matrix type organic EL display includes a plurality of anode lines, a plurality of cathode lines intersecting the anode lines, and a plurality of pixels, each including a light emission layer. The selection of one of the anode lines and one of the cathode lines cause light emission of a pixel located at the intersection of the selected signal lines.

[0007] The active matrix type organic EL display includes a plurality of pixels, each including a switching transistor, a driving transistor, and a storage capacitor as well as an anode, a cathode, and a light emission layer. The EL display further includes a plurality of gate lines transmitting gate signals and a plurality of data lines transmitting data voltages. The switching transistor is connected to one of the gate lines and one of the data lines and transmits the data voltage from the data line in response to the gate signal. The driving transistor receives the data voltage from the switching transistor and drives a current having a magnitude determined depending on the difference between the data voltage and a predetermined voltage such as a supply voltage. The current from the driving transistor enters the light emission layer to cause light emission having an intensity depending on the current. The storage capacitor is connected between the data voltage and the supply voltage to maintain their voltage difference. The gray scaling of the active matrix type EL display is accomplished by controlling the data voltages to adjust the current driven by the driving transistor. The color representation of the EL display is obtained by providing red, green and blue light emission layers.

[0008] In the meantime, the decrease of the supply voltage reduces the current driven by the driving transistors such that the displayed image is darker than is expected. For example, the data voltages with higher magnitude for displaying higher grays experience higher voltage drop such that the reduction of the currents driven by the driving transistors is much severer. The smaller currents makes the

pixels associated therewith emit darker lights, thereby generating cross-talk, which becomes severer as the number of the pixels expected to emit bright lights is increased.

SUMMARY OF THE INVENTION

[0009] A motivation of the present invention is to solve the above-described problems.

[0010] According to an aspect of the present invention, an organic electro-luminescence display panel is provided, which includes: an insulating substrate; a polysilicon layer formed on the substrate; a first insulating layer formed on the polysilicon layer; a gate wire formed on the first insulating layer; a second insulating layer formed on the gate wire; a data wire formed on the second insulating layer and including first and second portions; a pixel electrode connected to the first portion of the data wire; a partition defining an area on the pixel electrode; an organic light emitting member formed in the area on the pixel electrode; a common electrode formed on the light emitting member; and a planar supply voltage electrode disposed between the pixel electrode and the substrate and connected to the second portion of the data wire.

[0011] The supply voltage electrode may be disposed directly on the substrate.

[0012] The organic electro-luminescence display panel may further include a blocking layer formed on the substrate. The blocking layer may have an opening exposing a portion of the supply voltage electrode, the first and the second insulating layers may have a contact hole exposing the exposed portion of the supply voltage electrode through the opening, and the second portion of the data wire may be connected to the supply voltage electrode through the opening and the contact hole. The opening may be larger than the contact hole.

[0013] The polysilicon layer may include first and second transistor portions, each including a channel region, a source region, and a drain region, the gate wire may include first and second gate electrodes overlapping the first and the second transistor portions, respectively, and the data wire may include a first source electrode connected to the source region of the first transistor portion, a first drain electrode connected to the drain region of the first transistor portion and the second gate electrode, a second source electrode connected to the source region of the second transistor portion and the supply voltage electrode, and a second drain electrode connected to the drain region of the second transistor portion and the pixel electrode.

[0014] The polysilicon layer may further include a storage electrode region connected to the source region of the second transistor portion and the gate wire further comprises a storage electrode overlapping the storage electrode region and connected to the second gate electrode.

[0015] The pixel electrode may be formed of the same layer or the same material as the data wire.

[0016] The organic electro-luminescence display panel may further include an auxiliary electrode connected between the supply voltage electrode and the second source electrode. The auxiliary electrode may include the same layer as the gate wire.

[0017] The partition preferably includes black photoresist.

[0018] The pixel electrode may be opaque and the common electrode may be transparent. Alternatively, the pixel electrode is transparent and the common electrode is opaque.

[0019] When the pixel electrode is transparent, the supply voltage electrode preferably has a transmitting portion facing the light emitting member for transmitting light from the light emitting member.

[0020] The supply voltage electrode preferably has an opening facing at least a portion of the polysilicon layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawings in which:

[0022] **FIG. 1** is a layout view of an organic EL display panel according to an embodiment of the present invention;

[0023] **FIG. 2** is a sectional view of the organic EL display panel shown in **FIG. 1** taken along the line II-II';

[0024] **FIG. 3** is a sectional view of the organic EL display panel shown in **FIG. 1** taken along the line III-III';

[0025] **FIG. 4A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a first step of a manufacturing method thereof according to an embodiment of the present invention;

[0026] **FIGS. 4B and 4C** are sectional views of the organic EL display panel shown in **FIG. 4A** taken along the lines IVB-IVB' and IVC-IVC', respectively;

[0027] **FIG. 5A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 4A-4C**;

[0028] **FIGS. 5B and 5C** are sectional views of the organic EL display panel shown in **FIG. 5A** taken along the lines VB-VB' and VC-VC', respectively;

[0029] **FIG. 6A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 5A-5C**;

[0030] **FIGS. 6B and 6C** are sectional views of the organic EL display panel shown in **FIG. 6A** taken along the lines VIB-VIB' and VIC-VIC', respectively;

[0031] **FIG. 7A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 6A-6C**;

[0032] **FIGS. 7B and 7C** are sectional views of the organic EL display panel shown in **FIG. 7A** taken along the lines VIIIB-VIIIB' and VIIC-VIIC', respectively;

[0033] **FIG. 8A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 7A-7C**;

[0034] **FIGS. 8B and 8C** are sectional views of the organic EL display panel shown in **FIG. 8A** taken along the lines VIIIB-VIIIB' and VIIC-VIIC', respectively;

[0035] **FIG. 9A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 8A-8C**;

[0036] **FIGS. 9B and 9C** are sectional views of the organic EL display panel shown in **FIG. 9A** taken along the lines IXB-IXB' and IXC-IXC', respectively;

[0037] **FIG. 10A** is a layout view of the organic EL display panel shown in **FIGS. 1-3** in a step following the step shown in **FIGS. 9A-9C**;

[0038] **FIGS. 10B and 10C** are sectional views of the organic EL display panel shown in **FIG. 10A** taken along the lines XB-XB' and XC-XC', respectively;

[0039] **FIG. 11** is a layout view of a bottom emission type organic EL display panel according to an embodiment of the present invention;

[0040] **FIG. 12** is an exemplary sectional view of the display panel shown in **FIG. 11** taken along the line XII-XII';

[0041] **FIG. 13** is an exemplary sectional view of the display panel shown in **FIG. 11** taken along the line XIII-XIII';

[0042] **FIG. 14** is another exemplary sectional view of the display panel shown in **FIG. 11** taken along the line XIII-XIII'; and

[0043] **FIG. 15** is another exemplary sectional view of the display panel shown in **FIG. 11** taken along the line XIII-XIII'.

DETAILED DESCRIPTION OF EMBODIMENTS

[0044] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

[0045] In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region, substrate or panel is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0046] Then, organic electroluminescence display devices and manufacturing methods thereof according to embodiments of the present invention will be described with reference to the accompanying drawings.

[0047] First, an organic EL display according to an embodiment of the present invention is described in detail with reference to **FIGS. 1-3**.

[0048] **FIG. 1** is a layout view of an organic EL display panel according to an embodiment of the present invention, **FIG. 2** is a sectional view of the organic EL display panel shown in **FIG. 1** taken along the line II-II', and **FIG. 3** is a sectional view of the organic EL display panel shown in **FIG. 1** taken along the line III-III'.

[0049] A supply voltage electrode **112** supplied with a predetermined voltage such as a supply voltage is formed on an insulating substrate **110** preferably made of transparent glass or silicon wafer. The supply voltage electrode **112** is

preferably made of a conductive material having low resistivity such as Al, Al alloy, Ag, or Ag alloy and it substantially covers an entire surface of the substrate 110 to have a planar shape without having a stripe shape.

[0050] A blocking layer 111 preferably made of silicon oxide or silicon nitride is formed on the supply voltage electrode 112.

[0051] A polysilicon layer including a plurality of pairs of a first transistor portion 150a for a switching thin film transistor (TFT) and a second transistor portion 150b for a driving TFT is formed on the blocking layer 111.

[0052] The first transistor portion 150a includes a plurality of impurity regions such as a (first) source region 153a, an intermediate region 152a, and a (first) drain region 155a, which are doped with n type impurity and separated from one another, and a plurality of intrinsic regions such as a pair of (first) channel regions 154a disposed between the impurity regions 153a, 152a and 155a. The first source region 153a extends to form a storage electrode region 157.

[0053] The second transistor portion 150b includes a plurality of impurity regions such as a (second) source region 153b and a (second) drain region 155b, which are doped with p type impurity, and an intrinsic region such as a (second) channel region 154b disposed between the impurity regions 153b and 155b.

[0054] Alternatively, the impurity regions 153a, 152a and 155a of the first transistor portion 150a are doped with p type impurity, while the impurity regions 153b and 155b of the second transistor portion 150b are doped with n type impurity, depending on driving conditions.

[0055] A gate insulating layer 140 preferably made of silicon oxide or silicon nitride is formed on the polysilicon layer 150a and 150b.

[0056] A plurality of gate lines 121 including a plurality of pairs of first gate electrodes 123a and a plurality of second gate electrodes 123b, which are preferably made of low resistivity material such as Al or Al alloy, are formed on the gate insulating layer 140. Each pair of first gate electrodes 123a are branched from the gate line 121 and they intersect the first transistor portion 150a such that they overlap the pair of the first channel regions 154a. Each second gate electrode 123b is separated from the gate line 121 and it intersects the second transistor portion 150b such that it overlaps the second channel region 154b. The second gate electrode 123b extends to form a storage electrode 133 overlapping the storage electrode region 157 of the polysilicon layer 150a and 150b to form a storage capacitor.

[0057] A first interlayer insulating film 801 is formed on the gate lines 121 and the first and the second gate electrodes 123a and 123b.

[0058] A plurality of data lines 171, each including a plurality of first source electrodes 173a, a plurality of second source electrodes 173b, and a plurality of first and second drain electrodes 175a and 175b are formed on the first interlayer insulating film 801.

[0059] Each first source electrode 173a is branched from the data line 171 and connected to the first source region 153a through a contact hole 181 penetrating the first interlayer insulating film 801 and the gate insulating layer 140.

Each first drain electrode 175a is connected to the first drain region 155a through a contact hole 182 penetrating the first interlayer insulating film 801 and the gate insulating layer 140. The first drain electrode 175a is also connected to the second gate electrode 123b through a contact hole 183 penetrating the first interlayer insulating film 801 and the gate insulating layer 140.

[0060] Each second source electrode 173b has an island shape and it is connected to the second source region 153b through a contact hole 184 penetrating the first interlayer insulating film 801 and the gate insulating layer 140. Each second drain electrode 175b is connected to the second drain region 155b through a contact hole 186 penetrating the first interlayer insulating film 801 and the gate insulating layer 140. The second source electrode 173b is also connected to the supply voltage electrode 112 through a contact hole 187 penetrating the first interlayer insulating film 801, the gate insulating layer 140, and the blocking layer 111.

[0061] A second interlayer insulating film 802 is formed on the data lines 171, the source electrodes 173a and 173b, and the drain electrodes 175a and 175b. The second interlayer insulating film 802 is preferably made of silicon nitride, silicon oxide, or organic insulating material and it has a plurality of contact holes 185 exposing the second drain electrodes 175b.

[0062] A plurality of pixel electrodes 190 are formed on the second interlayer insulating film 802. Each pixel electrode 190 is connected to the second drain electrode 175b through the contact hole 185 and it is preferably made of reflective opaque material such as Al or Ag alloy. However, the pixel electrode 190 may be formed of a transparent conductive material such as ITO (indium tin oxide) and IZO (indium zinc oxide). The pixel electrode 190 may be incorporated with the second drain electrode 175b for reducing the manufacturing cost.

[0063] A partition 803 for separating pixels of the organic EL display panel is formed on the second interlayer insulating film 802 and the pixel electrodes 190. The partition 803 surrounds the pixel electrodes 190 like a bank to define depressions filled with organic light emitting material. The partition 803 is preferably made of organic insulating material and, more preferably, made of a photosensitive material containing black pigment, which is exposed to light and developed, such that the partition 803 functions as a light blocking member and a manufacturing method thereof is simplified.

[0064] A plurality of light emitting members 70 are formed on the pixel electrodes 190 and disposed in the depressions defined by the partition 803. The light emitting members 70 are preferably made of organic material emitting primary-color lights such as red, green and blue lights. The red, green and blue light emitting members 70 are arranged periodically.

[0065] A buffer layer 804 is formed on the light emitting members 70 and the partition 803. The buffer layer 804 may be omitted if it is not required.

[0066] A common electrode 270 supplied with a predetermined voltage is formed on the buffer layer 804. The common electrode 270 is preferably made of transparent conductive material such as ITO and IZO. If the pixel

electrodes **190** are transparent, the common electrode **270** is preferably made of reflective opaque metal such as Al.

[0067] An auxiliary electrode (not shown) made of low resistivity material is optionally provided for compensating the conductivity of the common electrode **270**. The auxiliary electrode may be disposed between the common electrode **270** and the buffer layer **804** or on the common electrode **270**, and it preferably has a matrix form and is disposed along the partition **803** such that it does not overlap the light emitting member **70**.

[0068] In the above-described organic EL display panel, the first transistor portion **150a**, the first gate electrode **123a** connected to the gate line **121**, the first source electrode **153a** connected to the data line **171**, and the first drain electrode **155a** form a switching TFT. In addition, the second transistor portion **150b**, the second gate electrode **123b** connected to the first drain electrode **155a**, the second source electrode **153b** connected to the supply voltage electrode **112**, and the second drain electrode **155b** connected to the pixel electrode **190** form a driving TFT. Furthermore, the pixel electrode **190** and the common electrode **270** serve as an anode and a cathode, respectively, and the storage electrode region **157** connected to the first drain region **155a** and the storage electrode **133** connected to the supply voltage electrode **112** through the second source electrode **153b** form a storage capacitor.

[0069] The switching TFT transmits the data voltage from the data line **171** to the driving TFT in response to the gate signal from the gate line **121**. Upon the receipt of the data voltage, the driving TFT generates a current having a magnitude depending on the difference between the data voltage and the supply voltage. In addition, the data voltage is charged in the storage capacitor to be maintained after the switching TFT is turned off. The current driven by the driving TFT enters into the light emitting member **70** through the pixel electrode **190** and reaches the common electrode **270**. The current flowing in the light emitting member **70** means that positive charge carriers such as holes and negative charge carriers such as electrons are injected into the light emitting member **70** from the anode **190** and the cathode **270**, respectively, and they are drifted by an electric field generated by the voltage difference between the anode **190** and the cathode **270**. The holes and the electrons in the light emitting member **70** then meet each other to be recombined into excitons, which emit light with a predetermined wavelength. The intensity of the emitted light depends on the current driven by the driving TFT and flowing in the light emitting member **70**.

[0070] The emitted light goes out of the display panel after passing through the common electrode **270** or the pixel electrode **190**. A transparent common electrode **270** and an opaque pixel electrode **190** are applicable to a top emission type EL display, which displays an image on its top surface. On the contrary, a transparent pixel electrode **190** and an opaque common electrode **270** are applicable to a bottom emission type EL display, which displays an image on its bottom surface. In the former case, the supply voltage electrode **112** can have various positions or arrangements between the light emitting members **70** and the substrate **111**. In the latter case, the supply voltage electrode **112** may be transparent at least in part in order to transmit the light emitted from the light emitting members **70**.

[0071] As described above, since the supply voltage electrode **112** has a planar shape covering the entire surface of the organic EL display panel, the magnitude of the supply voltage applied to the pixels is almost constant. In addition, since the supply voltage electrode **112** has a sheet resistance, a voltage drop may not significantly differentiate the magnitude of the supply voltage applied to the pixels. Therefore, a cross-talk resulted from the difference in the brightness between the pixels is significantly reduced.

[0072] Now, a method of manufacturing the organic EL display panel shown in FIGS. 1-3 is described with reference to FIGS. 4A-10C as well as FIGS. 1-3.

[0073] FIGS. 4A, 5A, 6A, 7A, 8A, 9A and 10A are layout views of the organic EL display panel shown in FIGS. 1-3 in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention, FIGS. 4B, 5B, 6B, 7B, 8B, 9B and 10B are sectional views of the organic EL display panels shown in FIGS. 4A, 5A, 6A, 7A, 8A, 9A and 10A taken along the lines IVB-IVB', VB-VB', VIB-VIB', VIIB-VIIB', VIIIB-VIIIB', IXB-IXB', and XB-XB', respectively, and FIGS. 4C, 5C, 6C, 7C, 8C, 9C and 10C are sectional views of the organic EL display panels shown in FIGS. 4A, 5A, 6A, 7A, 8A, 9A and 10A taken along the lines IVC-IVC', VB-VC', VIC-VIC', VIIC-VIIC', VIIIC-VIIIC', IXC-IXC', and XC-XC', respectively.

[0074] Referring to FIGS. 4A-4C, a conductive material is deposited on an insulating substrate **110** to form a supply voltage electrode **112**. The supply voltage electrode **112** may be photo-etched to form openings or transmitting portions therein.

[0075] A blocking layer **111** preferably made of silicon oxide is formed on an insulating substrate **110**, and an amorphous silicon layer is deposited on the blocking layer **111**. The deposition of the amorphous silicon layer is preferably performed by LPCVD (low temperature chemical vapor deposition), PECVD (plasma enhanced chemical vapor deposition) or sputtering. Consecutively, the amorphous silicon layer is laser-annealed to be crystallized into a polysilicon layer.

[0076] Next, the polysilicon layer is photo-etched to form a plurality of pairs of first and second transistor portions **150a** and **150b**.

[0077] Referring to FIGS. 5A-5C, a gate insulating layer **140** is deposited on the polysilicon layer **150a** and **150b**.

[0078] Successively, a gate metal layer is deposited on the gate insulating layer **140** and a photoresist film is coated, exposed to light, and developed to form a first photoresist PR1. The gate metal layer is etched by using the first photoresist PR1 as an etch mask to form a plurality of gate electrodes **123b** including storage electrodes **133** and a plurality of gate metal members **120**. P type impurity is injected into exposed portions of the second transistor portions **150b** of the polysilicon layer to form a plurality of P type impurity regions **153b** and **155b**. At this time, the first transistor portions **150a** of the polysilicon layer are covered with the first photoresist PR1 and the gate metal members **120** to be protected from impurity implantation.

[0079] Referring to FIGS. 6A-6C, the first photoresist PR1 is removed and another photoresist film is coated, exposed to light, and developed to form a second photoresist PR2.

The gate metal layer **120** is etched by using the first photoresist **PR2** as an etch mask to form a plurality of gate lines **121** including gate electrodes **123a**. N type impurity is injected into exposed portions of the first transistor portions **150a** of the polysilicon layer to form a plurality of N type impurity regions **153a** and **155a**. At this time, the second transistor portions **150b** of the polysilicon layer are covered with the second photoresist **PR2** to be protected from impurity implantation.

[0080] Referring to FIGS. 7A-7C, a first interlayer insulating film **801** is deposited on the gate lines **121** and the gate electrodes **123a** and **123b**. The first interlayer insulating film **801**, the gate insulating layer **140**, and the blocking layer **111** are photo-etched to form a plurality of contact holes **181**, **182**, **184** and **186** exposing the impurity regions **153a**, **155a**, **153b** and **155b**, respectively, as well as a plurality of contact holes **183** and **187** exposing the gate electrodes **123b** and portions of the supply voltage electrode **112**.

[0081] Referring to FIGS. 8A-8C, a data metal layer is deposited and photo-etched to form a plurality of data lines **171** including first source electrodes **173a**, a plurality of second source electrodes **173b**, a plurality of first and second drain electrodes **175a** and **175b**.

[0082] Referring to FIGS. 9A-9C, a second interlayer insulating film **802** is deposited on the data lines **171**, the source electrodes **173a** and **173b**, and the drain electrodes **175a** and **175b** as well as on the first interlayer insulating film **801**. The second interlayer insulating film **802** is photo-etched to form a plurality of contact holes **185** exposing the second drain electrodes **175b**.

[0083] Referring to FIGS. 10A-10C, a transparent conductive material or a low resistivity reflective material is deposited and patterned to form a plurality of pixel electrodes **190**. When the pixel electrodes **190** are made of reflective opaque material, they may be formed of the data metal layer along with the data lines **171**.

[0084] Referring to FIGS. 1-3, an organic film containing black pigment is coated on the pixel electrodes **190** and the second interlayer insulating film **802**, and it is exposed to light and developed to form a partition **803** defining a plurality of depressions on the pixel electrodes **190**. Thereafter, a plurality of organic light emitting members **70** are formed in the depressions by deposition or inkjet printing following a masking. The organic light emitting member **70** preferably has a multi-layered structure.

[0085] Next, an organic conductive material is deposited on the light emitting members **70** to form a buffer layer **804**, and ITO or IZO is deposited on the buffer layer **804** to form a common electrode **270**.

[0086] An auxiliary electrode (not shown) made of low resistivity material such as Al may be formed before or after the formation of the common electrode **270**.

[0087] As described above, a top emission type organic EL display panel according to this embodiment includes an opaque pixel electrode and a transparent common electrode **270**, and it displays an image on its top surface. The supply voltage electrode **112** can be placed on another position under the organic light emitting member **70**.

[0088] Next, a bottom emission type organic EL display panel including a transparent pixel electrode and an opaque

common electrode for displaying an image on its bottom surface is described in detail with reference to FIGS. 11-15.

[0089] FIG. 11 is a layout view of a bottom emission type organic EL display panel according to an embodiment of the present invention and FIGS. 12 and 13 are exemplary sectional views of the display panel shown in FIG. 11 taken along the lines XII-XII' and XIII-XIII', respectively.

[0090] As shown in FIGS. 11-13, a structure of an organic EL display panel according to this embodiment is similar to that shown in FIGS. 1-3.

[0091] In detail, a supply voltage electrode **112** and a blocking layer **111** are sequentially formed on an insulating substrate **110**. A polysilicon layer including a plurality of pairs of a first transistor portion **150a** for a switching TFT and a second transistor portion **150b** for a driving TFT is formed on the blocking layer **111**, and a gate insulating layer **140** is formed thereon. The first transistor portion **150a** includes a plurality of impurity regions such as a first source region **153a**, an intermediate region **152a**, and a first drain region **155a**, and a pair of first channel regions **154a** disposed between the impurity regions **153a**, **152a** and **155a**. The second portion **150b** includes a second source region **153b**, a second drain region **155b**, and a second channel region **154a** disposed between the second source region **153b** and the second drain region **155a**. A plurality of gate lines **121** including first gate electrodes **123a** and a plurality of second gate electrodes **123b** including storage electrodes **133** are formed on the gate insulating layer **140**, and a first interlayer insulating film **801** is formed thereon. A plurality of data lines **171** including first source electrodes **173a**, a plurality of second source electrodes **173b**, and a plurality of first and second drain electrodes **175a** and **175b** are formed on the first interlayer insulating film **801**, and a second interlayer insulating film **802** is formed thereon. A plurality of pixel electrode **190** and a partition **803** defining a plurality of depressions on the pixel electrodes **190** are formed on the second interlayer insulating film **802**, and a plurality of organic light emitting member **70** are formed in the depressions on the pixel electrodes **190**. A buffer layer **804** is formed on the organic light emitting members **70** and the partition **803**, and a common electrode **270** is formed on the buffer layer **804**.

[0092] The pixel electrodes **190** are transparent while the common electrode **270** is opaque. The supply voltage electrode **112** has a plurality of transmitting portions **T** facing the pixel electrodes **190** for the transmission of light emitted from the light emitting members **70**. In addition, the supply voltage electrode **112** has a plurality of openings **S** facing the channel regions **154a** of the first transistor portions **150a** for minimizing the effect of a supply voltage on the switching TFTs.

[0093] A manufacturing method of the organic EL display panel shown in FIGS. 11-13 according to an embodiment of the present invention forms the openings **S** and the transmitting portions **T** by patterning the supply voltage electrode **112** using a photolithography process after depositing the supply voltage electrode **112**.

[0094] The area of the transmitting portions **T** of the planar supply voltage electrode **112** according to this embodiment can be increased compared with a conventional linear supply voltage electrode.

[0095] FIG. 14 is another exemplary sectional view of the display panel shown in FIG. 11 taken along the lines XIII-XIII'.

[0096] Referring to FIG. 14, a plurality of auxiliary members 127 for compensating the connection between the supply voltage electrode 112 and the second source electrodes 173b are formed on the gate insulating layer 140. The auxiliary members 127 are connected to the supply voltage electrode 112 through contact holes 147 penetrating the gate insulating layer 140 and the blocking layer 111, and also connected to the second source electrodes 173b through contact holes 187 penetrating the first interlayer insulating film 801. The auxiliary members 127 are preferably made of the same layer as the gate lines 121.

[0097] FIG. 15 is another exemplary sectional view of the display panel shown in FIG. 11 taken along the lines XIII-XIII'.

[0098] Referring to FIG. 15, the blocking layer 111 has a plurality of openings 117 exposing the supply voltage electrode 112 and a plurality of contact holes 187 penetrating the first interlayer insulating film 801 and the gate insulating layer 140 and having smaller size than the openings 117 are formed in the openings 117. The second source electrodes 173b are connected to the supply voltage electrodes 112 through the contact holes 187.

[0099] Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present invention, as defined in the appended claims.

What is claimed is:

1. An organic electro-luminescence display panel comprising:

- an insulating substrate;
- a polysilicon layer formed on the substrate;
- a first insulating layer formed on the polysilicon layer;
- a gate wire formed on the first insulating layer;
- a second insulating layer formed on the gate wire;
- a data wire formed on the second insulating layer and including first and second portions;
- a pixel electrode connected to the first portion of the data wire;
- a partition defining an area on the pixel electrode;
- an organic light emitting member formed in the area on the pixel electrode;
- a common electrode formed on the light emitting member; and
- a planar supply voltage electrode disposed between the pixel electrode and the substrate and connected to the second portion of the data wire.

2. The organic electro-luminescence display panel of claim 1, wherein the supply voltage electrode is disposed directly on the substrate.

3. The organic electro-luminescence display panel of claim 1, further comprising a blocking layer formed on the substrate.

4. The organic electro-luminescence display panel of claim 3, wherein the blocking layer has an opening exposing a portion of the supply voltage electrode, the first and the second insulating layers have a contact hole exposing the exposed portion of the supply voltage electrode through the opening, and the second portion of the data wire is connected to the supply voltage electrode through the opening and the contact hole.

5. The organic electro-luminescence display panel of claim 4, wherein the opening is larger than the contact hole.

6. The organic electro-luminescence display panel of claim 1, wherein the polysilicon layer comprises first and second transistor portions, each including a channel region, a source region, and a drain region, the gate wire comprises first and second gate electrodes overlapping the first and the second transistor portions, respectively, and the data wire comprises a first source electrode connected to the source region of the first transistor portion, a first drain electrode connected to the drain region of the first transistor portion and the second gate electrode, a second source electrode connected to the source region of the second transistor portion and the supply voltage electrode, and a second drain electrode connected to the drain region of the second transistor portion and the pixel electrode.

7. The organic electro-luminescence display panel of claim 6, wherein the polysilicon layer further comprises a storage electrode region connected to the source region of the second transistor portion and the gate wire further comprises a storage electrode overlapping the storage electrode region and connected to the second gate electrode.

8. The organic electro-luminescence display panel of claim 7, wherein the pixel electrode is formed of the same layer or the same material as the data wire.

9. The organic electro-luminescence display panel of claim 7, further comprising an auxiliary electrode connected between the supply voltage electrode and the second source electrode.

10. The organic electro-luminescence display panel of claim 9, wherein the auxiliary electrode comprises the same layer as the gate wire.

11. The organic electro-luminescence display panel of claim 1, wherein the partition comprises black photoresist.

12. The organic electro-luminescence display panel of claim 1, wherein the pixel electrode is opaque and the common electrode is transparent.

13. The organic electro-luminescence display panel of claim 1, wherein the pixel electrode is transparent and the common electrode is opaque.

14. The organic electro-luminescence display panel of claim 1, wherein the pixel electrode is transparent and the supply voltage electrode has a transmitting portion facing the light emitting member for transmitting light from the light emitting member.

15. The organic electro-luminescence display panel of claim 1, wherein the supply voltage electrode has an opening facing at least a portion of the polysilicon layer.

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摘要(译)

根据本发明的一个方面，提供了一种有机电致发光显示板，包括：绝缘基板；形成在基板上的多晶硅层；形成在多晶硅层上的第一绝缘层；栅极线形成在第一绝缘层上；形成在栅极线上的第二绝缘层；数据线形成在第二绝缘层上并包括第一和第二部分；像素电极连接到数据线的第二部分；限定像素电极上的区域的分区；有机发光构件形成在像素电极上的区域中；形成在发光元件上的公共电极；平面电源电压电极，设置在像素电极和基板之间，并连接到数据线的第二部分。

